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Applicants John W. Rapp, Larry Jackson, Mark Jones, and Troy Cherasaro

Title:

PIPELINE ACCELERATOR FOR IMPROVED COMPUTING ARCHITECTURE AND RELATED SYSTEM AND METHOD

Serial Number:

10/683,929

Filing Date:

October 9, 2003

Examiner/Unit:

/ 2818

Attorney Docket No.:

1934-13-3

CERTIFICATE OF MAILING OR TRANSMISSION

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TO THE COMMISSIONER FOR PATENTS:

In compliance with 37 CFR § 1.56 and § 1.97, Applicants acting by and through the attorney of record, hereby discloses patents and other documents listed on the attached Form PTO-1449 which may be considered relevant to the examination of the subject application.

A copy of the cited non-U.S. reference is enclosed.

Certification Under Section 1.97(e)

Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this statement.

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

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| Complete if Known | | |
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| Application Number | 10/683,929 | |
| Filing Date | October 9, 2003 | |
| First Named Inventor | John W. Rapp | |
| Art Unit | 2818 | |
| Examiner Name | | |
| Attorney Docket Number | 1934-13-3 | |

| | NON PATENT LITERATURE DOCUMENTS | NON PATENT LITERATURE DOCUMENTS | | | | |
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| | BAKSHI S; GAJSKI D D; "Partitioning and Pipelining for Performance-Constrained Hardware/Software Systems", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 7, NR. 4, PG. 419-432, (1999-12-00), XP000869229 | | | | | |
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|-----------|---------------------------------------|------------|--|
| Examiner | | Date | |
| Signature | | Considered | |

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